Session 32 Overview

PLLs, VCOs, and Dividers

Chair: Ian Galton, University of California, San Diego, La Jolla, California

Associate Chair: Takehiko Nakao, Toshiba, Kawasaki, Japan

Phase locked loops (PLLs) are critical blocks in virtually all solid-state electronic systems. They frequently determine overall system performance in applications such as cellular radio and high-speed serial communications, and are essential for clock generation in system-on-a-chip (SoC) applications. For example, the phase noise from the RF PLL in a cellular telephone receiver mixes with interfering signals and corrupts the desired signal, so the ability of the receiver to reject interference depends critically on the PLL phase noise.

As communication and storage standards evolve toward higher frequencies and higher bandwidths, the performance limitations of PLLs become increasingly critical. PLLs frequently must be integrated with large digital blocks so there is strong and increasing pressure to implement high-performance PLLs in highly-scaled CMOS technology. The 9 papers in this session present several PLLs and PLL components that incorporate techniques to overcome various analog circuit limitations of highly scaled CMOS technology.

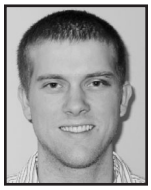
The first five papers present PLLs. Paper 32.1 describes a VHF synthesizer PLL with a high division ratio that does not require an off-chip loop filter and is insensitive to PVT variations. Paper 32.2 presents a 2.5GHz ring-oscillator-based PLL that incorporates techniques to improve power supply rejection and $1/f$ noise performance. Paper 32.3 presents a PLL that generates a 63-phase selectable clock for a DVD write system. It utilizes a compact coupled ring oscillator structure to achieve 32ps phase resolution. Paper 32.4 demonstrates an enhancement based on multiple delayed PFDs and charge pumps to reduce reference spurs. Paper 32.5 presents a 6.25GHz LC-oscillator-based PLL that achieves $0.55ps_{rms}$ jitter from a 1V supply. It demonstrates a new charge pump that addresses problems associated with low-voltage CMOS processes including leakage current and reduced headroom.

The last four papers present critical PLL components. Paper 32.6 demonstrates an 11.4GHz distributed VCO consisting of 12 coupled negative g_m cells to generate 24 clock phases with direction control. Papers 32.7 and 32.8 demonstrate extremely high-frequency CMOS divide-by-4 circuits based on different techniques that each provide new high-water marks in performance. The circuit presented in Paper 32.7 incorporates static and dynamic dividers. It has an input frequency of 40GHz and a power consumption of 3mW. The circuit presented in Paper 32.8 is a harmonic injection locked divider with an input frequency of 70GHz and a power consumption of 2.75mW. Paper 32.9 demonstrates a divide-by-3 injection-locked divider circuit with an input frequency of 16-18GHz and an extended tuning range relative to previous injection locked divide-by-3 circuits.

 1-4244-0079-1/06/$20.00

32.1 A PVT-Tolerant Low-1/f-Noise Dual-Loop Hybrid PLL in 0.18µm CMOS **1:30 PM**
H-R. Lee, Seoul National University, Seoul, Korea

A dual-loop analog-digital hybrid PLL with a small-bandwidth digital loop and large-bandwidth analog loop achieves low jitter by suppressing 1/f noise and does not require off-chip loop filter components. The operating range using a narrow-range VCO is from 10 to 200MHz. The output jitter over this range is <0.028UI_{pp}. The chip is implemented in a 0.18µm CMOS process and consumes 50mW from a 1.8V supply.



32.2 A 0.5 to 2.5GHz PLL with Fully Differential Supply-Regulated Tuning **2:00 PM**
M. Brownlee, Oregon State University, Corvallis, OR

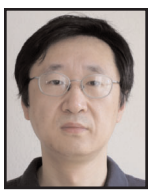
A PLL uses a fully differential supply-regulated tuning scheme to combat power-supply noise. The charge pump uses a resistor to set the current and reduce the flicker noise corner. Fabricated in a 0.18µm CMOS process, the PLL area is 0.15mm^2. Operating at 2.4GHz, it has 3.29ps_{rms} jitter, a frequency range of 0.5 to 2.5GHz, and draws 14mA from a 1.8V supply.

32.3 A PLL for a DVDx16 Write System with 63 Output Phases and 32ps Resolution **2:30 PM**
S. Dosho, Matsushita Electric, Moriguchi, Japan

A current-controlled oscillator (CCO) with 32ps phase resolution is realized by coupling ring oscillators in a 65nm CMOS process. A compact layout method achieves 36×46$µm^2$ area and multiphase outputs whose timing errors are small. A CCO with 63 output phases is used in the PLL for a DVDx16 write system. The measured DNL of the output phases is within 1.0LSB at 490MHz.

32.4 A Spur Suppression Technique for Phase-Locked Frequency Synthesizers **3:15 PM**
T-C. Lee, National Taiwan University, Taipei, Taiwan

A 4.8GHz integer-*N* frequency synthesizer with distributed phase-frequency detectors and charge pumps moves spurious tones to higher frequencies and reduces the spur levels. PPM is used to relax the analog circuit accuracy requirement. The circuit is fabricated in a 0.18µm CMOS technology, dissipates 18mW from a 1.8V supply and suppresses sidebands by 10dB.



32.5 A 6.25GHz 1V LC-PLL in 0.13µm CMOS **3:45 PM**
R. Gu, Texas Instruments, Dallas, TX

A 6.25GHz PLL with integrated LC-tank VCO, on-chip loop filter and quadrature outputs is fabricated in 0.13µm CMOS technology. Operated at 1V supply with 62.5MHz input reference clock frequency, an output clock jitter of 0.5ps_{rms} is achieved by using a charge pump with rail-to-rail operation and leakage-current cancellation.

32.6 A Reversible Poly-Phase Distributed VCO **4:15 PM**
N. Tzartzanis, Fujitsu, Sunnyvale, CA

A reversible 24-phase closed-loop distributed VCO is implemented in 90nm 10M triple-well 1.2V CMOS using co-planar transmission lines as delay elements. The measured tuning range is 10.4 to 11.4GHz, the phase noise is -96.65dBc/Hz at 1MHz offset, and the circuit uses 70mW from a 1.2V supply.

32.7 A Combined Dynamic and Static Frequency Divider for a 40GHz PLL in 80nm CMOS **4:30 PM**
G. von Büren, ETH Zürich, Zürich, Switzerland

A divide-by-4 circuit operates for input frequencies from 31 to 41GHz at signal amplitudes ≤0.5V_{pp}. The circuit consists of a dynamic followed by a static frequency divider. The dynamic and static frequency dividers consume 2mA and 1mA, respectively, from a 1.1V supply.

32.8 70GHz CMOS Harmonic Injection-Locked Divider **4:45 PM**
K. Yamamoto, University of Tokyo, Kashiwa-shi, Japan

A 70GHz CMOS harmonic injection-locked divider (HILD) is presented, where a third-harmonic mixer is realized by a differential-voltage-driven MOSFET. The chip is fabricated in a 6M 90nm CMOS process. A maximum operating frequency of 71.6GHz with a locking range of 12% at a supply voltage of 0.5V is measured. The chip consumes 2.75mW.

32.9 An 16-to-18GHz 0.18µm Epi-CMOS Divide-By-3 Injection-Locked Frequency Divider **5:00 PM**
H. Wu, University of Rochester, Rochester, NY

A new injection-locked frequency divider (ILFD) topology is proposed for divide-by-odd-number operation. A 18 GHz divide-by-3 prototype is implemented using 0.18µm standard digital CMOS with low-resistivity substrate. It achieves 1GHz locking range with 3.4dBm injection power, which increases to 3.2GHz with built-in tuning. The phase noise is close to theoretical value of 9.5dB down from input.